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A frequency hopping synchronization system.

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Monterey, California

THESIS

A FREQUENCY HOPPING SYNCHRONIZATION SYSTEM

by

Robert John McDevitt

December 1980

Thesis Advisor: G. A. Myers

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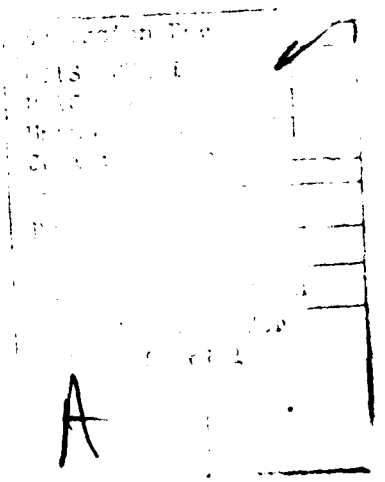

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A Frequency Hopping Synchronization System

by

Robert John McDevitt
Lieutenant Commander, United States Navy
B.S., United States Naval Academy, 1969

Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

Frequency hopping is one of several spread spectrum communications techniques which offer some immunity to jamming as well as some rejection of multipath interference. Synchronization of the frequency hopping transmitter and receiver is necessary in an operating system. This research concerns a method of synchronization whereby the receiver resynchronizes with the transmitter once each frequency hopping cycle. Thus, in most applications clock drift becomes negligible and continuity of data recovery is ensured. This report presents the principles and details of circuit design and operation.

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I. INTRODUCTION

Spread spectrum communications systems have been growing rapidly in popularity and practicality in recent years, especially for military applications. To date, most military schemes have been of the direct sequence type. Frequency Hopping (FH) does not provide the direct sequence advantage of covertness. FH does provide decreased susceptibility to interference. Also, FH may be an attractive communications technique where multipath reception occurs (urban areas).

Most spread spectrum systems require the receiver to be synchronized with the transmitter. This report presents the results of research on a particular FH synchronization system. Chapter II presents the principle of FH and describes the synchronization technique considered in this work. Chapter III contains a block diagram of the experimental system and presents the design details. Results and conclusions appear in Chapter IV.

II. PRINCIPLES OF FREQUENCY HOPPING

The basic principle of frequency hopping is the generation of multiple carrier frequencies in a random fashion. By expanding the frequency band of operation in this way, the probability of being jammed can be decreased.

In a conventional frequency modulated (FM) transmitter shown in Fig. 1, the data frequency modulates a carrier which is then up converted (sometimes) and amplified. The superheterodyne receiver of Fig. 2 uses a local oscillator signal to translate the received carrier to an intermediate frequency for filtering and amplification before data recovery (demodulation). In the frequency hopping transmitter (Fig. 3), the carrier frequency is caused to vary (hop) over a certain frequency range and at a certain rate (hops per second) by using a mixer and a frequency synthesizer which create the hopping frequency. Before demodulating the incoming frequency hopping signal, the frequency hopping receiver (Fig. 4) removes the hop pattern by using a local oscillator which is hopping in a manner like that of the received signal. This requires that the receiver be synchronized with the transmitter.

In direct sequence spread spectrum systems a chip rate much greater than the data rate is common and synchronization at the chip rate is required for correlator type receivers [1]. Since the hop rate approximates the data rate in FH systems, synchronization is less critical. This research

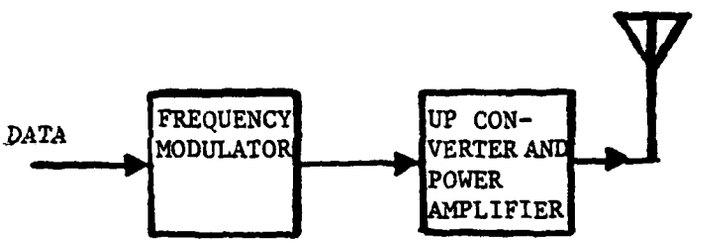


Figure 1. Block Diagram of a Conventional Radio Transmitter

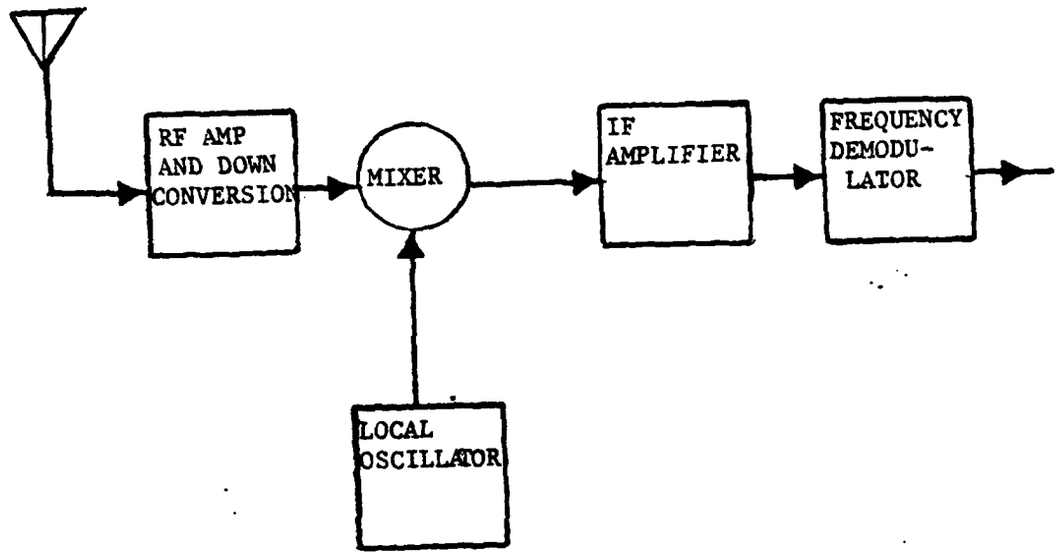


Figure 2. Block Diagram of a Super-heterodyne Receiver

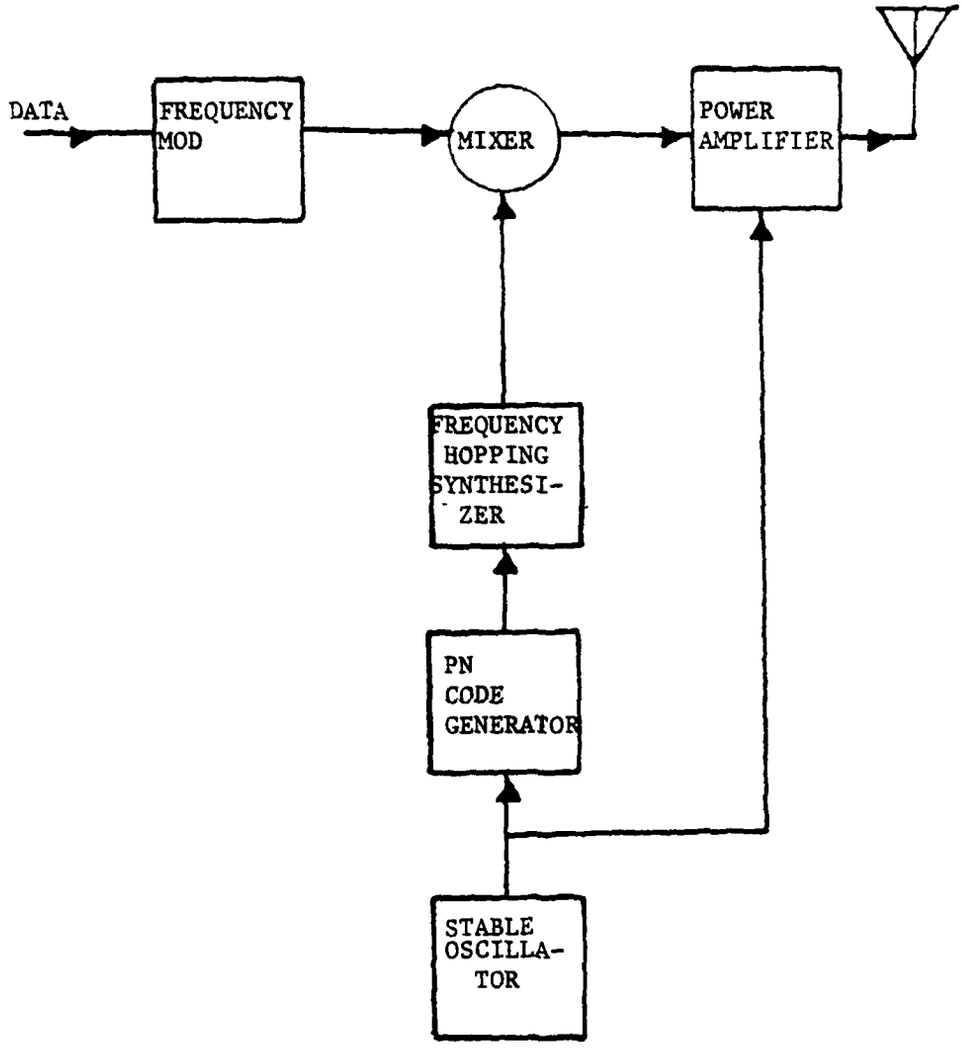


Figure 3. Block Diagram of a Frequency Hopping Transmitter

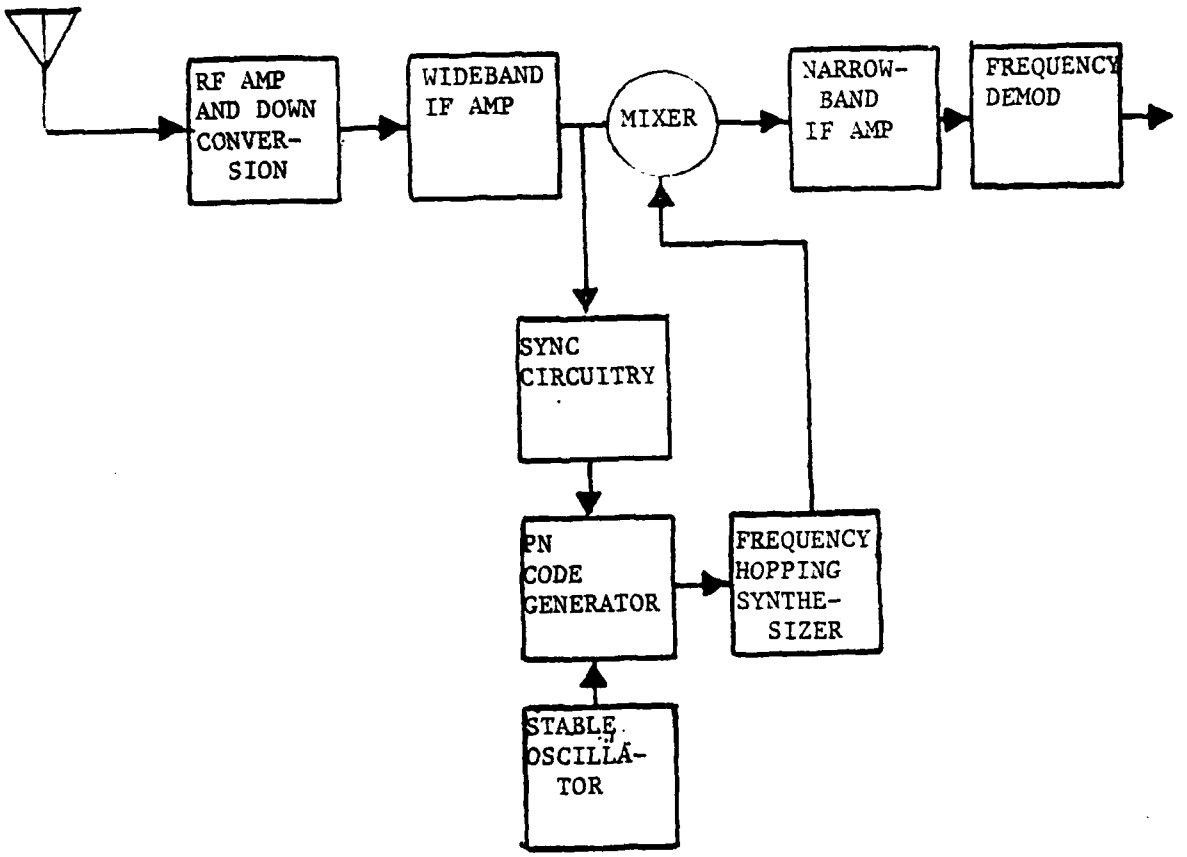


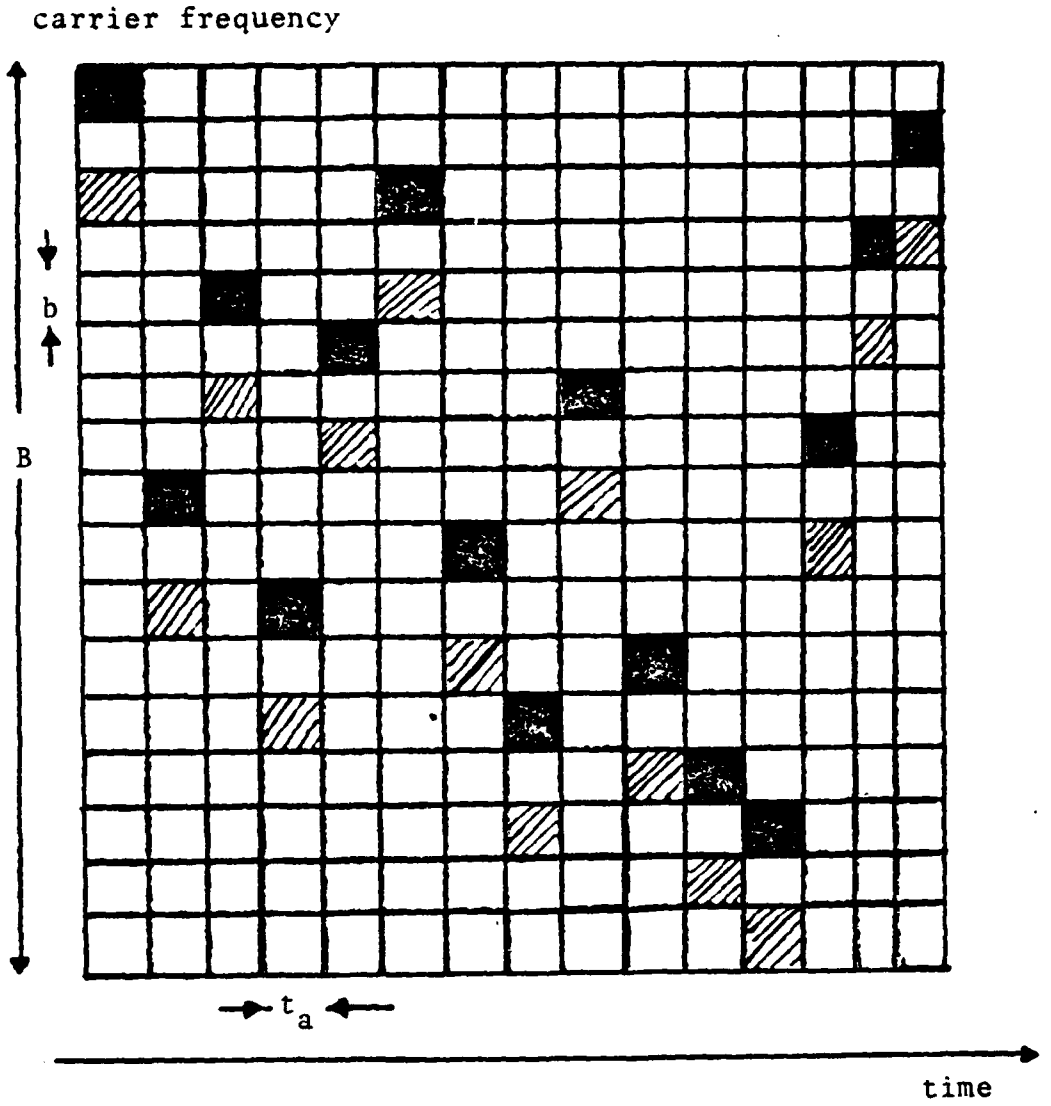
Figure 4. Block Diagram of a Frequency Hopping Receiver

considers a means of synchronizing the incoming signal once each cycle of the hop pattern. Consequently, clock drift becomes insignificant.

Fig. 5 is an example of a frequency hopping pattern. The transmitted signal occupies a frequency cell of width b hertz, which varies over a range of B hertz. The time cell of duration t_d seconds (dwell per hop) defines the hop rate = $\frac{1}{t_d}$ hops/sec. Typically, $\frac{1}{t_d}$ is also approximately the data rate (bits/sec). Data is transmitted in binary form by offsetting the hop frequency as shown in Fig. 5. This offset is provided by the frequency modulator in Fig. 3. The hopping range (B) depends on equipment and frequency availabilities. The bandwidth per hop (b) depends on the carrier modulation during the dwell time (t_d). A minimum value of b is $\frac{2}{t_d}$ hertz.

Frequency hopping can overcome interference from multipath effects. For example, let t_R = propagation time of the reflected signal and t_D = propagation time of the direct signal as shown in Fig. 6. Now, if $t_R - t_D > t_d$, then the receiver will have hopped (tuned) to a new frequency before the reflection arrives. This tuning blocks the reflected (multipath) signal.

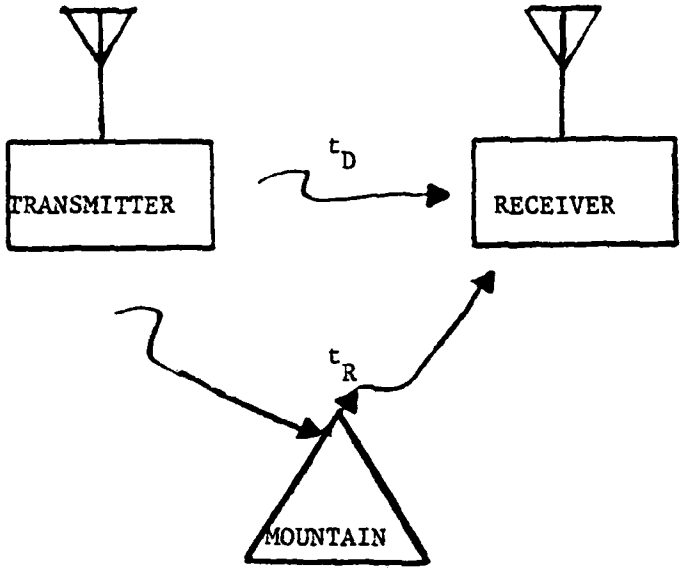
FH can also decrease the likelihood of being jammed. Consider the following argument where it is assumed there are many hops during each data bit:



t_d = dwell time per hop
B = hopping range in hertz
b = bandwidth per hop
PG = processing gain = B/b

■ = "1"
▨ = "0"

Figure 5. Frequency Hopping Time vs. Frequency Diagram



t_D = propagation time of direct signal

t_R = propagation time of reflected signal

Figure 6. Diagram of Multipath Effect Situation

Assume

N_h = The number of channels available to the frequency hopper

N_j = The number of channels jammed

n_k = The number of hops per data bit

n_e = The number of wrong hop decisions per data bit necessary to cause an error

With these assumptions,

p = error probability for a single trial

$= N_j/N_h$

$q = 1 - p$

The probability of error P(E) is

$$P(E) = \text{Prob}\{n_e \text{ hits in } n_K \text{ trials}\} + \text{Prob}\{n_e+1 \text{ hits in } n_K \text{ trials}\} + \ldots + \text{Prob}\{n_K \text{ hits in } n_K \text{ trials}\}$$

This is the same probability of n_e heads in n_K trials in a coin toss experiment. Using the binomial expansion:

$$P(E) = \sum_{K=n_e}^{n_K} \binom{n_K}{K} p^K q^{n_K-K}$$

For example, let $n_K = 3$, $n_e = 2$, $N_j = 1$, $N_h = 100$ and $p = 10^{-3}$. Then,

$$P(E) = \sum_{K=2}^{3} \binom{3}{K} p^K q^{3-K} = 3 \times 10^{-6}$$

By increasing the number of hops per data bit from one to three the probability of error was decreased by a factor of 10^{-3}.

Interference from repeater jammers can be avoided also by receiver tuning and appropriate selection of the dwell time per hop (t_d). As shown in Fig. 7, if $t_d < t_u + t_p + t_j - t_f$, then interference from jammers is rejected by receiver tuning. For variable geometry situations, a good solution is to use the shortest possible dwell time per hop.

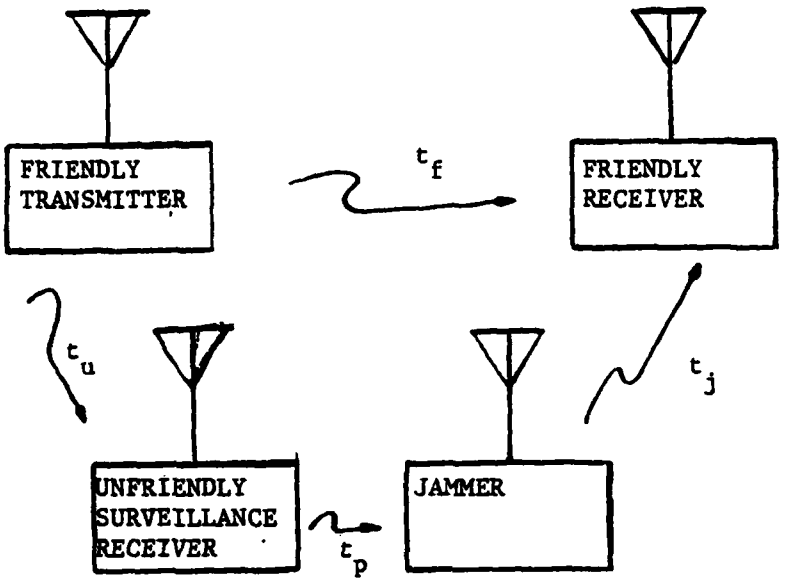


Figure 7. Diagram of Repeater Jammer Situation

III. CIRCUIT DESIGN AND OPERATION

A. TRANSMITTER

The transmitter design is a conventional one which uses a feedback shift register to generate random code words. These code words are converted to random hopping frequencies which are then used as shown in Fig. 8.

1. Feedback Shift Register (FSR)

The feedback shift register (FSR) of Fig. 9 generates a sequence of pseudo-random binary code words which determine the frequency to be transmitted. The feedback shift register's main component is a four bit parallel in parallel out (PIPO) shift register which is preloaded with a binary code word. When the first clock pulse arrives, that code word is transferred to the frequency synthesizer. Additionally, the outputs of stages 1 and 4 are applied to an exclusive or (XOR) gate whose output is applied to stage 1. There are 2^n-1 possible code words which can be generated using a FSR having n stages. (The all zeroes state repeats and so must be avoided.) In this work n = 4 and so 15 code words (frequency hops) can be generated.

2. Frequency Synthesizer

The frequency synthesizer accepts the fifteen random binary codes and converts them to fifteen frequencies. With each clock pulse the synthesizer hops to a new frequency. A hopping cycle consists of fifteen hops.

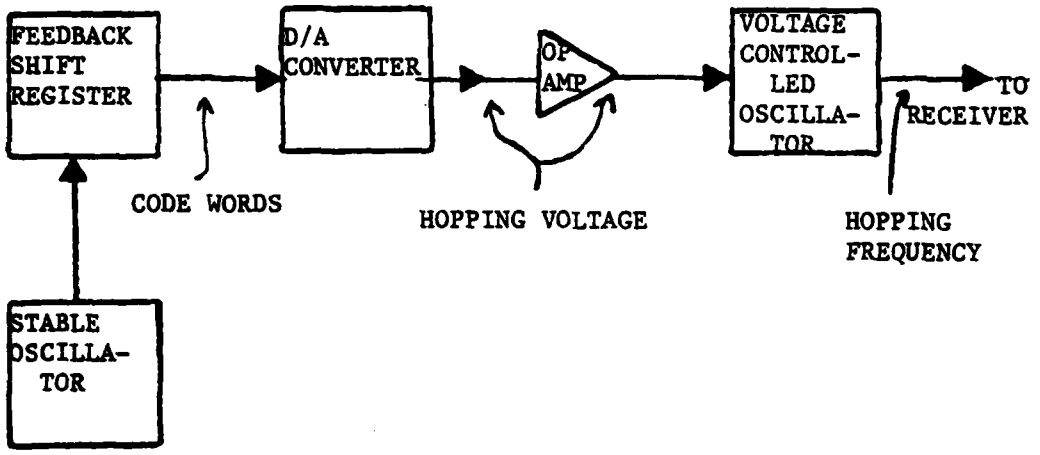


Figure 8. Frequency Hopping Transmitter Block Diagram

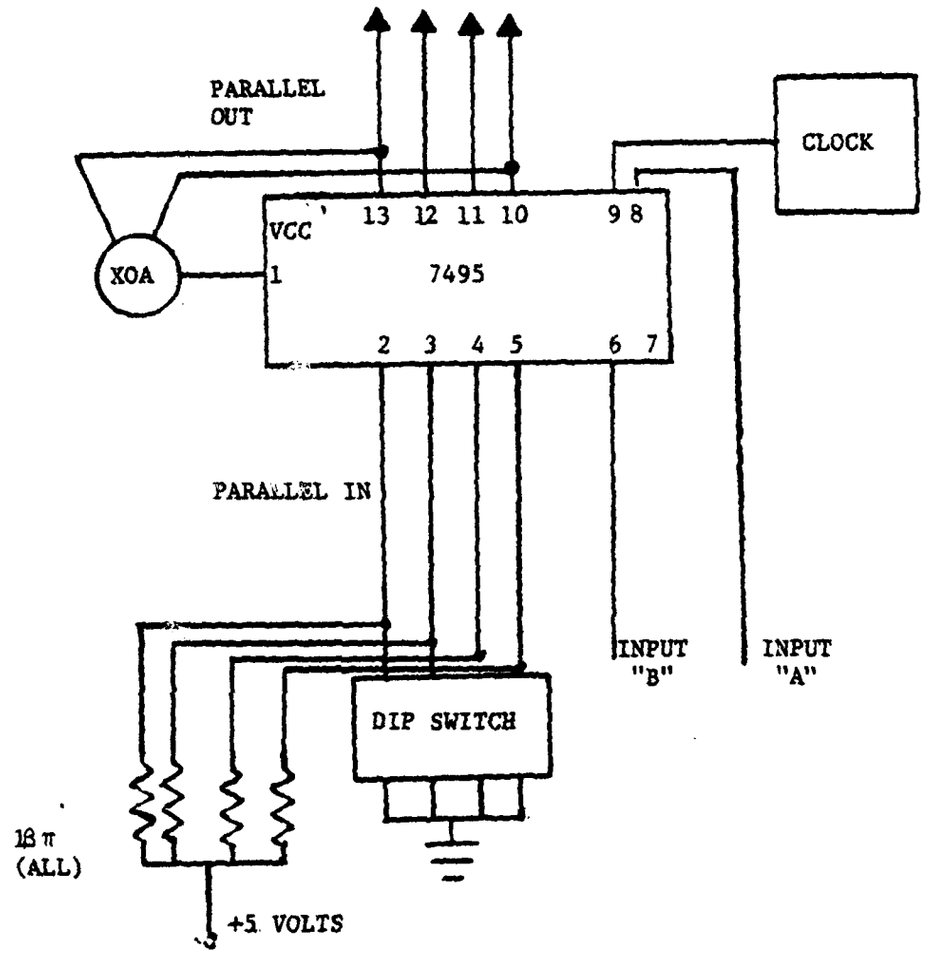


Figure 9. Feedback Shift Register Block Diagram

The frequency synthesizer (Fig. 10) consists of a digital/analog (D/A) converter, an opamp and a voltage controlled oscillator (VCO). The D/A converts each binary code into an analog voltage. The opamp ensures the input to the VCO is in the required voltage range. The VCO converts each DC voltage into a corresponding frequency. This hopping frequency when mixed with a fixed subcarrier frequency creates a random carrier frequency.

Fig. 11 is a time lapse photograph showing the first four hops of the hopping cycle. Details of the frequency synthesizer circuitry are in Appendix A.

B. RECEIVER

In this work, the frequency synthesizer output is routed directly to the receiver. The receiver design chosen and shown in Fig. 12 is a standard superheterodyne receiver whose local oscillator (LO) frequency hops synchronously with the transmitter's local oscillator frequency (Fig. 3).

The RF amplifier and wideband IF amplifier of Fig. 4 filter and convert the incoming signal to an appropriate frequency band which is then mixed with the hopping local oscillator frequency. In this experiment, the transmitter's frequency synthesizer output is assumed to be the same as the output of the wideband IF amp which is, then, the receiver input.

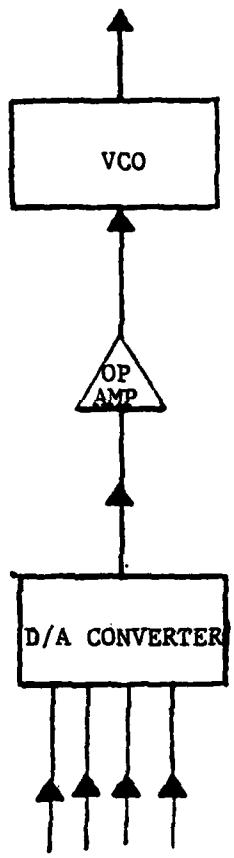


Figure 10. Frequency Synthesizer Block Diagram

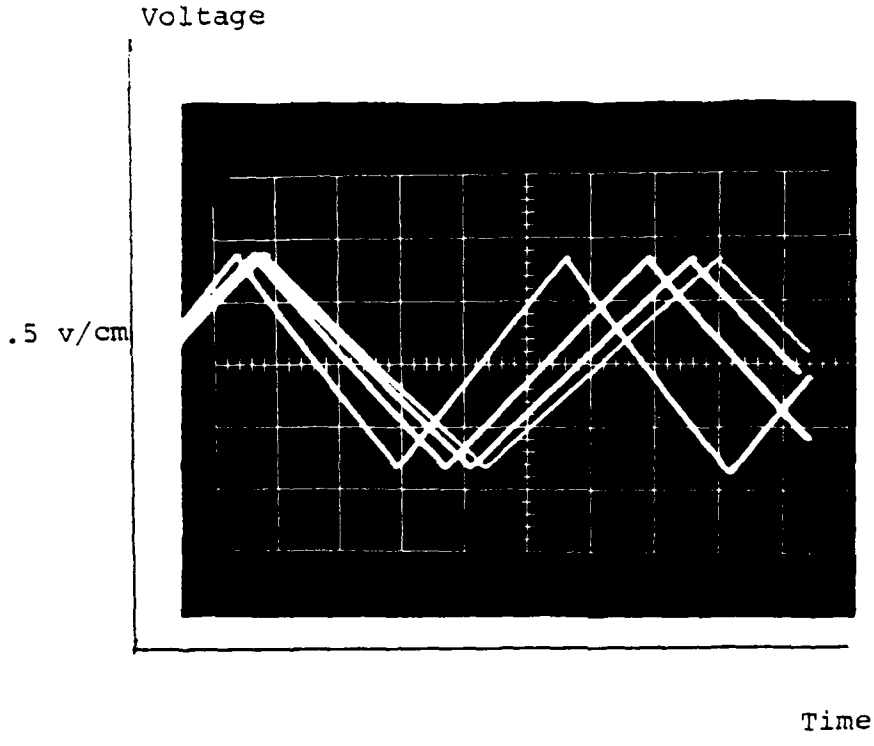


Figure 11. Time Lapse Photograph of First Four Hops of FH Cycle

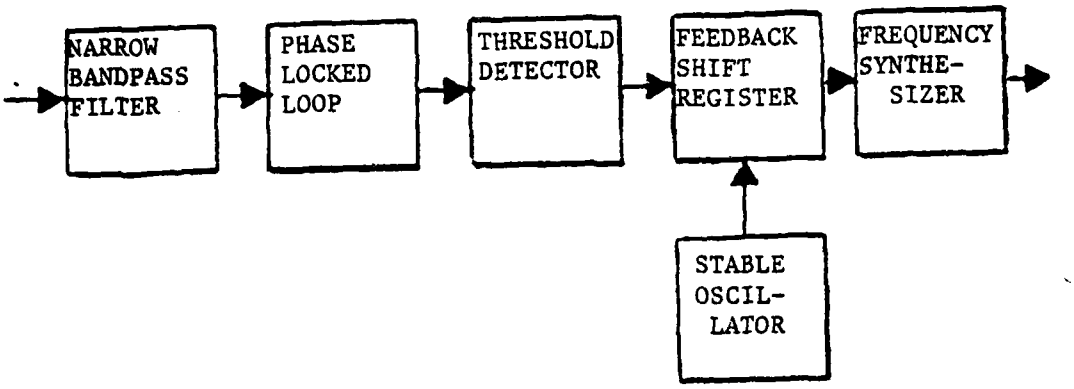


Figure 12. Frequency Hopping Receiver Block Diagram

1. Narrow Bandpass Filter

The narrow bandpass filter of Fig. 12 is a key element of the synchronization system. The filter is tuned to pass one of the frequencies in the set of 15 in the frequency hop pattern. In this manner the narrow bandpass filter output initiates the synchronizing process at the same point in each frequency hop cycle. This single detected frequency is converted to the DC voltage levels required to load, enable and clock the receiver's feedback shift register in synchronism with its counterpart in the transmitter.

Fig. 13 shows the filter's relative output at each hop. The largest signal is the single detected frequency and repeats every fifteen hops.

The narrow bandpass filter, the FLT U-2, is an active IC filter which provides a wide frequency range, a variable center frequency and a variable Q. Details of the circuitry are in Appendix B.

2. Phase Locked Loop

The phase locked loop detects, captures, and tracks the frequency hop selected by the narrow bandpass filter. The phase locked loop essentially generates a particular "DC" voltage level at a specific point in each frequency hop cycle.

The NE/SE 565 is a self contained IC phase locked loop which adapts to a variety of center frequencies. Details of the circuitry are in Appendix C.

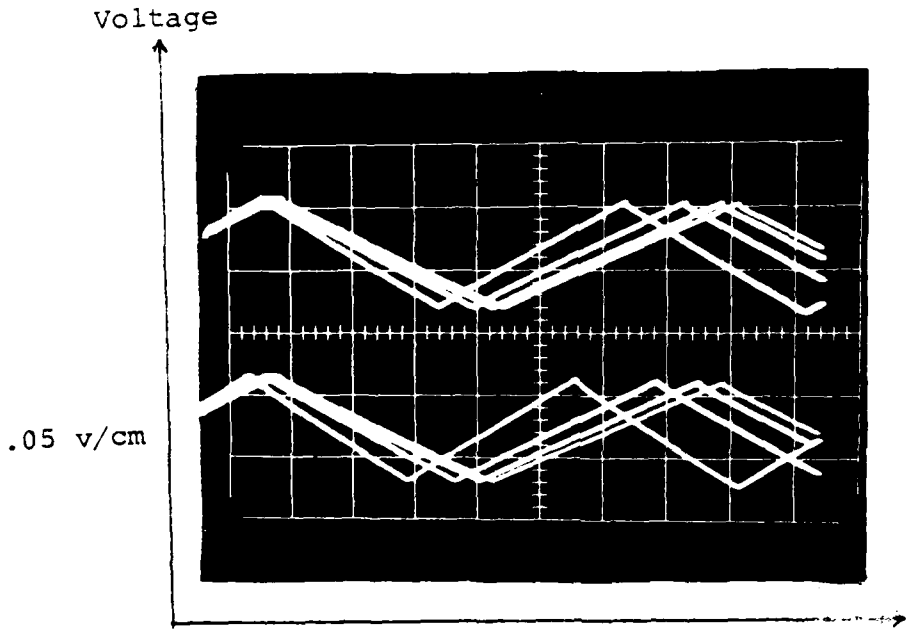


Figure 13. Narrow Band Pass Filter Output

3. Threshold Detector

A threshold circuit is used to detect the large voltage level of the phase locked loop output. The output of the threshold detector is used to load, enable and clock the receiver's feedback shift register. A network (Fig. 14) of voltage comparators, AND gates and inverters is employed to provide a successive pair of two simultaneous but inverse inputs required by the feedback shift register. When the prechosen frequency hop passes through the bandpass filter, the phase locked loop generates a large voltage level and the threshold detector sets input "A" to "1" and input "B" to "0". When the next hop arrives input "A" shifts to "0" and input "B" shifts to "1".

4. Feedback Shift Register (FSR)

Once every fifteen frequency hops, the threshold detector output "loads" the receiver FSR to an appropriate state. The FSR is then clocked through the hop cycle. The receiver FSR connections are the same as those of the transmitter FSR shown in Fig. 9. This procedure provides for resynchronizing the receiver every fifteen hops (L hops in general).

To avoid loss of data during the one hop loading process, a voltage comparator/OR gate is placed in parallel with the threshold detector. The comparator/OR gate output is applied directly to the frequency synthesizer's VCO, converting this output to a known voltage required by the VCO

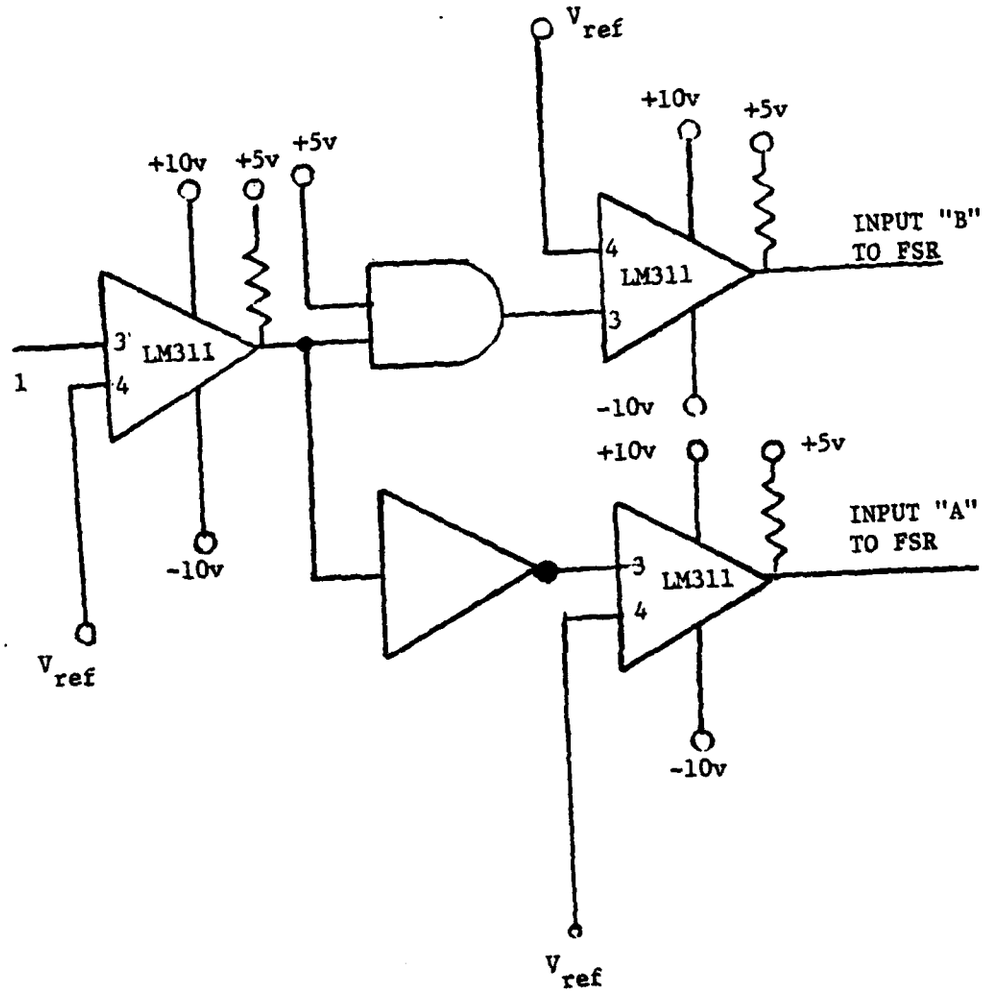


Figure 14. Block Diagram of the Threshold Detector Network

to generate the known frequency, thus provides continuity of data recovery.

5. Frequency Synthesizer

The frequency synthesizer consists of a digital/analog (D/A) converter, an opamp and a voltage controlled oscillator (VCO). The D/A converts the coded inputs from the feedback shift register into an analog voltage. The opamp amplifies the D/A output to the VCO's required voltage range. The VCO then converts the DC voltage to a triangle wave (not a sine wave because of the VCO design). In this manner, the frequency of the VCO output is made to correspond with that of the transmitter output. Figure 15 shows the first four hops of the receiver's frequency synthesizer (top) compared to the transmitter's (bottom).

Details of the receiver's frequency syntehsizer design are the same as those of the transmitter's found in Appendix A.

The output of the frequency hopping local oscillator is mixed with the frequency hopping incoming signal. When these two hopping cycles are synchronized, the mixer output is a constant frequency during a data bit. This frequency is offset (shifted or keyed) to represent the other binary data bit. Any one of various types of frequency demodulators can be used to recover the digital data from the frequency shift keyed (FSK) mixer output signal.

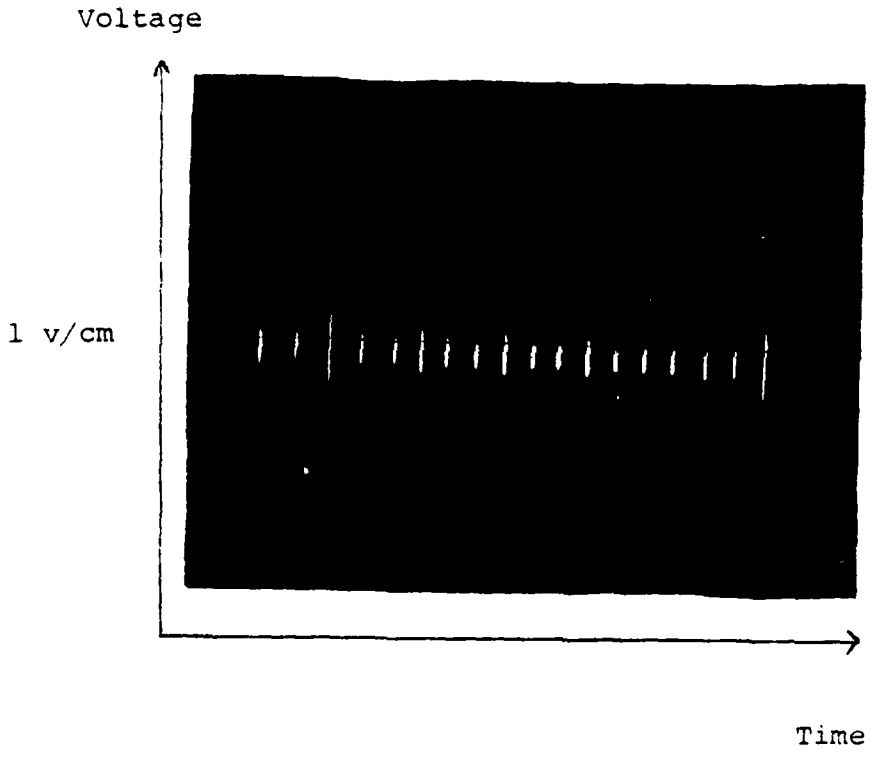


Figure 15. Transmitter/Receiver Frequency Synthesizer Output

IV. CONCLUSIONS/RECOMMENDATIONS

The circuitry operated as expected after some adjustments. The receiver synchronizing system will acquire and regenerate the received frequency hopping cycle.

The system does not require sensitive or precise circuitry. Its simplicity is an attractive feature when considering practical systems.

The narrow bandpass filter is a key circuit in the system design. Consequently, in the design of a practical system, the characteristics of this filter should be considered when specifying the number and spacing of the hops, data rate, etc.

APPENDIX A

FREQUENCY SYNTHESIZER

The frequency synthesizer circuit is shown in Fig. A-1. It was necessary to amplify the output of the D/A converter to meet the input voltage requirements of the VCO which were: $.75\,V^+ < V_{IN} < V^+$ i.e., 7.5 volts $< V_{IN} <$ 10. By using the opamp configuration shown $(V_{IN})_{MAX}$ = 8.9 volts and $(V_{IN})_{MIN}$ = 8.45 volts.

The external resistor and capacitor of the NE/SE 566 determined its free running frequency (f_o) as follows:

$$f_o \simeq \frac{2[V^+ - V_{IN}]}{R_1 C_1 V^+}$$

$$R_1 = 3.6\ K$$

$$C_1 = .1\ \mu f$$

$$f_o \simeq 8.6\ kHz$$

A list of code words with corresponding analog voltages and output frequencies is shown in Table A.1. The receiver code word 1010 is repeated as a result of the one hop loading process. However since the correct voltage is supplied by the voltage comparator/OR gate, the correct frequency $\simeq$ 10.05 kHz is generated by the VCO.

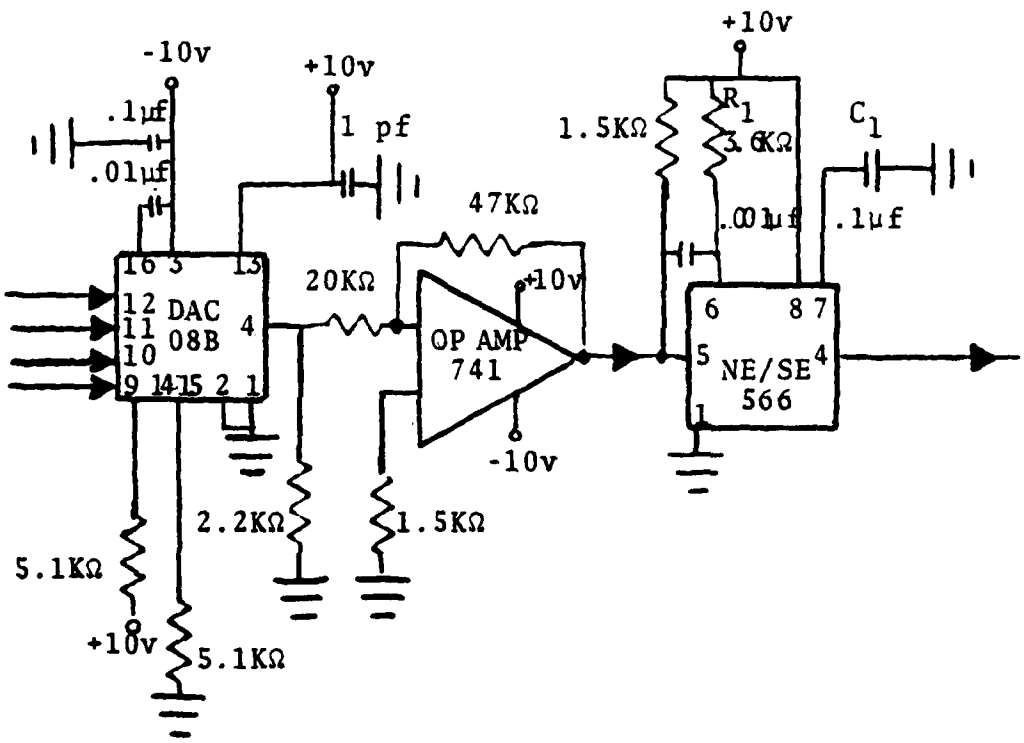


Figure A.1. Frequency Synthesizer Block Diagram

Table A.1

List of Code Words with Corresponding Frequencies

FSR_{OUT}	D/A_{OUT} (Volts)	VCO_{OUT} (kHZ)	FSR_{OUT}	D/A_{OUT} (Volts)	VCO_{OUT} (kHz)
0001	8.47	11.12	0001	8.45	10.80
1000	8.72	9.37	1000	8.69	9.10
1100	8.86	8.28	1100	8.82	8.21
1110	8.93	7.75	1110	8.88	7.81
1111	8.97	7.48	1111	8.90	7.66
0111	8.69	9.51	0111	8.64	9.50
1011	8.82	8.57	1011	8.77	8.57
0101	8.62	10.04	1010	8.75	10.05
1010	8.78	8.84	1010	8.85	8.69
1101	8.90	8.00	1101	8.62	8.02
0110	8.66	9.77	0110	8.72	9.63
0011	8.54	10.59	0011	8.50	10.39
1001	8.75	9.03	1001	8.71	8.96
0100	8.58	10.31	0100	8.55	10.23
0010	8.51	10.87	0010	8.48	10.53

APPENDIX B

NARROW BANDPASS FILTER

The FLT-U2 is a second-order state variable filter which uses three operational amplifiers. Its bandpass transfer function is:

$$H(S) = \frac{k\,S}{S^2 + \frac{\omega_o}{Q}S + \omega_o{}^2}$$

The necessary resistor values shown in Fig. B-1 are determined as follows:

$f_o \simeq 9.9\ K\Omega \pm 5\%$

$Q \simeq 719 \pm 5\%$

$R_1 = \text{open}$

$R_2 = 100\ K$

$R_3 = \frac{100\ K}{3.48\,Q - 1} = 40\ \Omega$

$R_4 = R_5 = \frac{5.03 \times 10^7}{f_o} = 4.99\ K\Omega$

$V^- = -10\ V$

$V^+ = +10\ V$

Due to the high value of Q it was necessary to isolate the filter with opamp buffers to prevent a change in filter

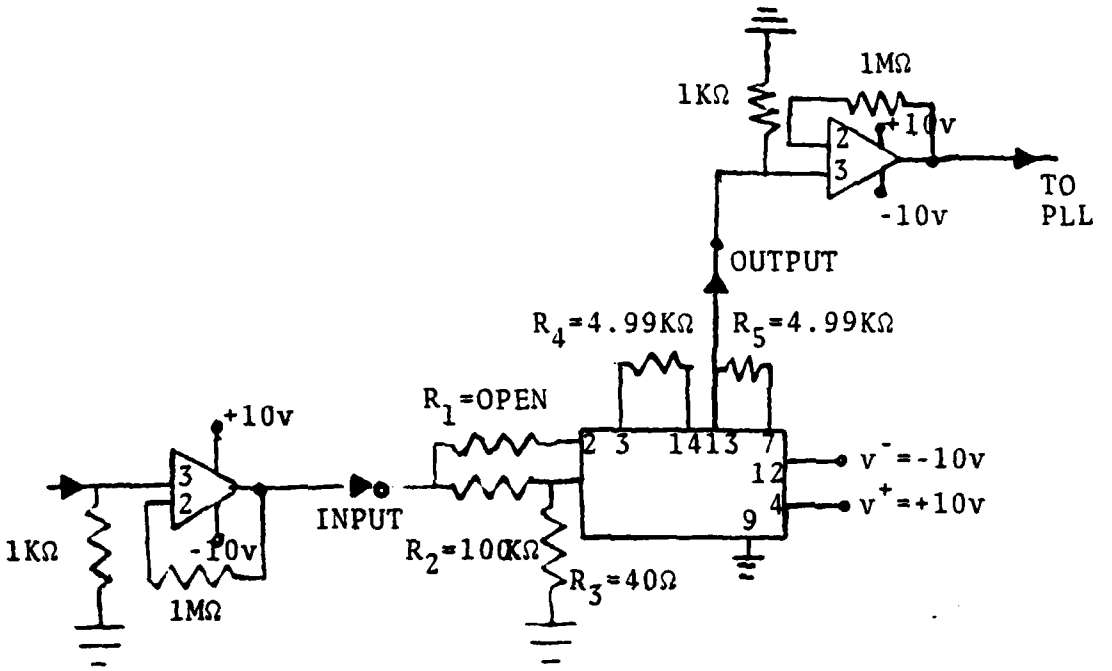


Figure B-1. Block Diagram of Narrow Bandpass Filter

characteristics as input and output impedances changed.

Fig. B-2 shows the filter's passband.

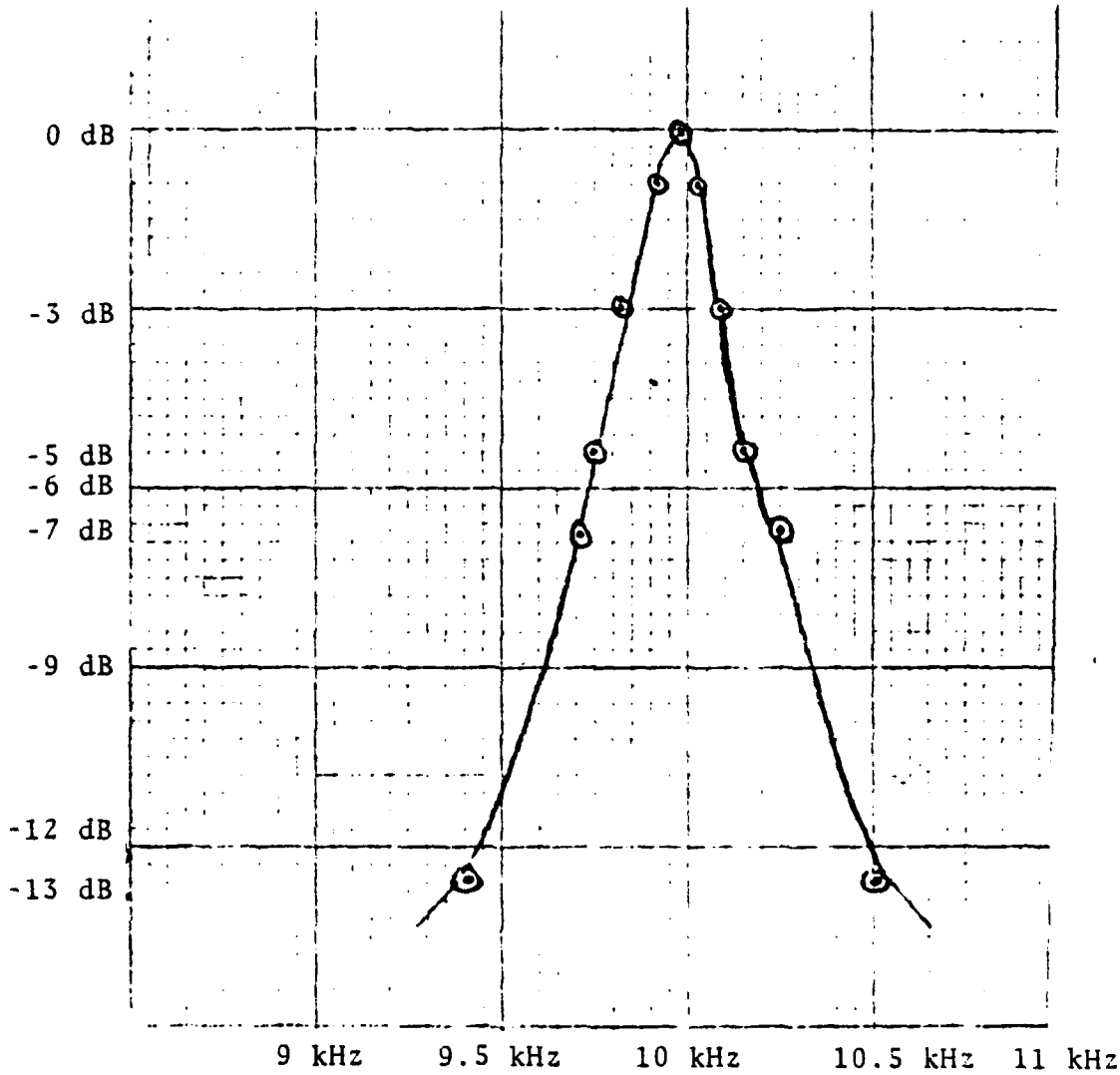


Figure B-2. Narrow Bandpass Filter Passband

APPENDIX C

PHASE LOCKED LOOP

The phase locked loop circuit is shown in Fig. C-1. The free running frequency (f_o), capture frequency (f_c) and lock frequency (f_i) calculations were made as follows:

$$V^+ = 10 \text{ V}$$

$$V^- = 10 \text{ V}$$

$$f_o \sim 9 \text{ kHz}$$

$$f_o = \frac{1.2}{4R_1C_1}$$

$$R_1C_1 = 3.3 \times 10^{-5}$$

Let $C_1 = 10^{-8} = .01 \ \mu f$

$$R_1 = 3.3 \ k\Omega$$

$$f_\ell = \frac{\pm 8 f_o}{V^+} = \pm .4 \ f_o = \pm 3600 \text{ Hz}$$

$$f_c = \pm \frac{1}{2\pi}\left[\frac{2\pi f_\ell}{\tau}\right]^{1/2}$$

$$\tau = 3.6 \times 10^{-3} \ C_2 \text{ (given)}$$

$$C_2 = .015 \ \mu f$$

$$f_c = \pm 40.8 \text{ kHz}$$

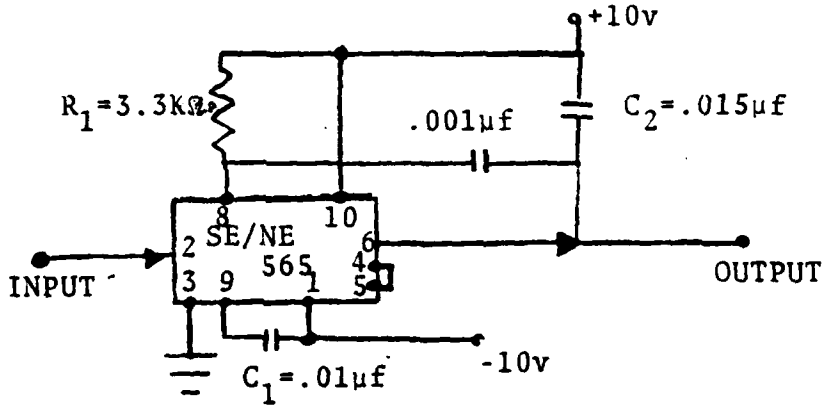


Figure C-1. Block Diagram of Phase Locked Loop

LIST OF REFERENCES

1. Dixon, R.C., Spread Spectrum Systems, John Wiley and Sons, 1976.

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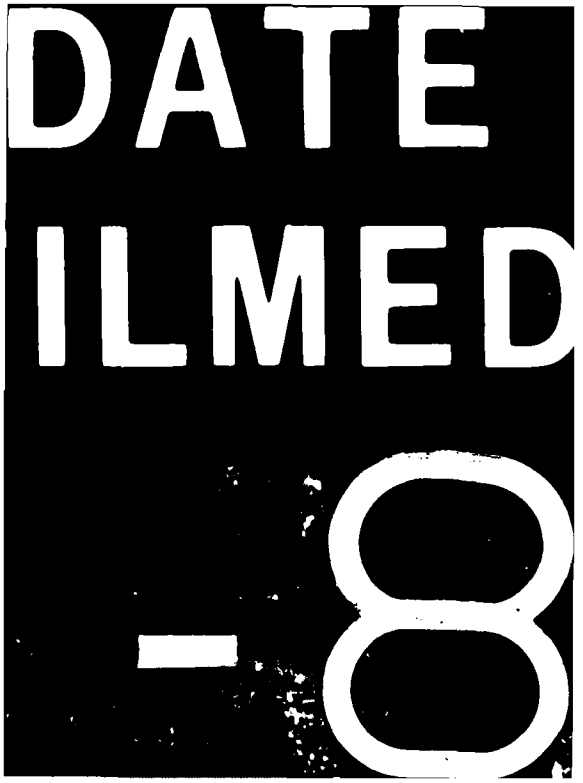
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